

FEDERAL UNIVERSITY OF TECHNOLOGY OWERRI

SCHOOL OF COMPUTING AND INFOTECHNOLOGY (SCIT), DEPARTMENT OF COMPUTER SCIENCE

RAIN SEMESTER EXAMINATIONS ON CSC/504: COMPUTER GRAPHICS; SESSION 2018/2019

INSTRUCTIONS: ANSWER ANY FOUR QUESTIONS; Time allowed: (2 1/2) Hours

QUESTION ONE.

- a) Give an annotated sketch of process control.
- b) Describe precisely in four statements the functional forms of process control.
- c) c) What makes process control an invaluable tool of management?
- d) Analogue computers provide real-time operations and fast solutions to some analytical problems but suffer from limitations in: (i)..... (ii)..... (iii).....
- e) State the features of hybrid computers.

Question Two

- (a) In ~~two~~<sup>one</sup> hundred and fifty words (150) describe precisely the applications of A/D and D/A devices.
- (b) Give the sketch of the operational amplifier used as an analogue adder
- (c) Give the four principal equations needed for the deduction of the equation:

$$-V_0 = V_1 * R_f/R_1 + V_2 * R_f/R_2$$

Question Three

What instruction formats would be suitable for programmed transfer I/O instructions:

- (a) If a single accumulator processor were used;
- (b) If a scratch-pad (RAM) is available and transfers are to be allowed involving any scratch-pad location?
- (c) Give the sketch of Two-bit, four-way demultiplexer.

Question Four

In DMA,

- (a) State the four principal information needed for data transfer.
- (b) Give the sketch of Bus-oriented DMA

Question Five

In DMA transfer operations, whenever the processor attempts to operate, a clash for main memory access occur from time to time. State exactly any **two** of the **three** options available to the designer to resolve the clashes of interest.

Question Six

- (a) Give a schematic diagram of request arbiter.
- (b) Give the four Failure logic models to arbitrate asynchronous service requests: (i) Failure model; (ii) wave forms; (iii) failure rate; (iv) cure.
- (c) Give the sketch of the routine for handling an interrupt.
- (d) The Interrupt hardware consists of logic to: i)....., ii)....., iii).....